REMARKS

Pending in the application are claims 1-17, of which claims 1, 2, 8 and 17 are independent. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance

Rejections to the Drawings Pursuant to 37 CFR 1.83(a)

The Examiner has rejected the drawings for failing to particularly point out all of the features described in the claims. Applicant respectfully submits an amended set of drawings which serve to identify each featured claimed within the pending application. Applicant additionally requests the cancellation of Figure 4 from the pending application. Applicant further submits that the features of claims 5, 6, 7,8,12 and 13 are depicted clearly in currently pending figures 6A and 6B. Applicant additionally submits that the compression of instructions in accordance with claims 12 and 13 is further depicted in pending figures 8A and 8B. In regards to elements disclosed in claims 14 – 17, Applicant submits that the Figures 7, 8A, and 8B details these elements in accordance with 37 CFR 1.83(a). In light of the newly submitted drawings, Applicant respectfully requests that he Examiner withdraw the rejection to the drawings.

Rejections to the Specification

The Examiner has rejected the Abstract for repeating information given in the title. In light of the Examiners objection to the abstract, Applicant respectfully submits an amended abstract. Applicant believes that the amended abstract addresses the Examiners objection and is in the proper format for inclusion in the pending application.

Applicant amends the title of the application in accordance with the Examiners proposed change, and additionally has removed all references to " a system" from the "Field of the invention" section of the application. Applicant has further deleted the embedded hyperlinks within the specification in accordance with the requirements of the MPEP. In light of such

changes, Applicant submits that the Examiners rejections to these informalities have been sufficiently overcome.

Regarding the Examiner's objection to the specification for failing to provide sufficient antecedent basis for the claimed subject matter, Applicant submits that the claims have been amended to address the lack of proper antecedent basis concerns. Addressing the Examiner's rejection to the subject matter of claim 4, which reads "rotating at least one instruction based at least in part on the number of valid instructions in the bundle" applicant respectfully submits amended claim 4, which now reads in part "shifting at least one instruction". Applicant submits that the amendment to claim 4 is fully supported by the specification and introduces no new matter to the pending application.

In regards to the Examiner's objection to the language of claim 5-7 and claims 12-13, which reads in part "compressing the bundle of instructions", Applicant respectfully submits that claims 5-7 and 12-13 are in condition for allowance. Applicant submits that the term "compressing" is well understood by one skilled in the applicable art, and used in accordance with the practice of those skilled in the art within the pending application. The term "compressing", as used in the pending application and noted by the Examiner in the pending office action, can be interpreted as the reduction in size of the instruction bundle. In light of this, Applicant respectfully requests that the Examiner pass claims 5-7 and 12-13 to allowance.

Claims 9 and 11 are further rejected by the Examiner on the basis that the term "bundling" lacks antecedent basis in the description. Applicant respectfully submits that the term bundling is understood by one of ordinary skill in the art to generally refer to the technique of gathering instructions together for use with the present invention. In the present invention, the term bundling, as used in the description, is directed toward the gathering of those instructions occurring prior to the complex instruction. In light of this, Applicant respectfully urges the Examiner to pass claims 9 and 11 to allowance.

Claim rejections under 37 CFR 1.75 (a)

Claims 1, 2 and 17 have been rejected as being vague and indefinite under 37 CFR 1.75(a). Applicant respectfully traverses these rejections. Applicant submits that the term "edge detecting valid instructions" is proper, and draws the Examiner's attention to paragraphs [0024]-[0026] of the present application wherein the technique of edge detection as applied to an instruction is detailed. Applicant therefore respectfully requests that the Examiner withdraw those rejections under 37 CFR 1.75(a) and pass claims 1,2 and 17 to allowance.

Applicant further submits that those claim informalities noted in the office action have been addressed and corrected, as evidenced herein.

Rejections Pursuant to 35 U.S.C. §112

The Examiner has rejected claims 6 and 13 for failing to point out and distinctly claim the subject matter which the applicant regards as his invention. In particular, the Examiner has objected to the term "monotonic instruction set" as being vague and lacking in antecedent basis. Applicant respectfully submits the term "monotonic instruction set" is well understood by those of ordinary skill in the art and is further defined within the pending specification. Citing paragraph [0020], Applicant submits that while addressing the instruction bundle evidenced in Figure 5, the tem "monotonically valid" is defined as:

> ""Monotonically" valid means that all the valid instructions 86, having their respective valid bit set high (or "1"), are at the front, or "top," of the instruction bundle 84. Any invalid instructions 90 having their respective valid bit set low (or "0"), are at the back, or the "bottom," of the instruction bundle 84."

In light of such language, Applicant submits that the monotonic instruction bundle terminology of claims 6 and 13 is readily understood by one of ordinary skill in the art and contains proper antecedent basis in accordance with 35 USC §112. Applicant therefore asks that Examiner to withdraw the rejection to claims 6 and 13 under 35 USC §112.

Rejections Pursuant to 35 U.S.C. §102(B)

The Examiner rejected claim 1 pursuant to 35 U.S.C. §102 (b) as being unpatentable over Sato et al. (US Patent No.: 4,566,103). Applicant respectfully traverses this rejection in light of the following arguments. Amended claim 1 recited *a method for calculating the number of valid instructions within a microprocessor* wherein instructions are advanced along a microprocessor pipeline and are edge detected to determine valid instructions within the microprocessor pipeline. Sato, in comparison is directed to the recovery from an error condition in a microprogram controlled unit. The Sato reference fails to recite the *calculation of the number of valid instructions within a microprocessor* as recited in amended claim 1. Furthermore, addressed in the cited language at column 4 lines 61-68 and column 5, lines 1-4, applicants submit that the circuit illustrated in Figure 3 fails to disclose the edge detection of valid instructions in accordance with amended claim 1 of the present invention but rather notes a generic error check circuit and error correcting circuit. In light of this, Applicants submit that the Sato patent fails to recite each element of pending amended claim 1, and therefore ask the Examiner to withdraw the rejections to Claim 1 under 35 U.S.C. §102(B)

Rejections Pursuant to 35 U.S.C. §103

The Examiner has rejected claims 1-5, 7-12 and 14-17 pursuant to 35 U.S.C. §103 as being unpatentable over Panwar et al. (U.S. Patent No. 6,098,165) in further view of Wakerly (Third Edition, Digital Design, Principles & Practices).

For the reasons set forth below, Applicants respectfully traverse these rejections.

Summary of Claimed Invention

The claimed invention relates to the calculating of the number of valid instructions within a microprocessor instruction bundle. The calculation of the number of these valid instructions can be determined using edge detection techniques. Furthermore, the instructions within the bundle may be monotonically arranged, namely arranged in a manner wherein the

order of the instructions are preserved. Furthermore, if dealing with instructions that are not monotonically arranged, the present invention can shift valid instructions to the top of the instruction bundle such that the valid instructions now lie onward from the first instruction slot within the bundle. Using such an arrangement, upon encountering an invalid instruction before a valid instruction, the invalid instruction will be considered valid, but will be marked "not executable." Using such an arrangement, only instructions after the last valid instruction within the bundle will be invalid. The number of valid instructions within the bundle may now be determined using the faster and simpler method of edge detection.

Summary of Panwar

Panwar discloses a method of processing complex and non-complex instructions without penalizing the processing of non-complex instructions. In effectuating this goal, initially makes complete instructions with a marker bit, and allows these instructions to bypass the existing instruction pipeline such that the pipeline used by non-complex instructions. A controller is used to scan the marked instructions in the main bundle, and break up the main bundle of instructions into a smaller bundle that contains only complex instructions. The non-complex instructions are then processed in a manner in which they bypass the helper logic of Panwar, while complex instructions are processed and expanded into microinstructions using the helper logic. Using such an arrangement, the core non-complex instructions are not burdened by the presence of multiple complex instructions in a wide-issue processor.

Summary of Wakerly

Wakerly discusses edged detection in a flip flop that combined two latches. The illustrated flip flop of Wakerly samples an input and changes its output upon detecting the rising or falling edge of a controlling signal. As illustrated in figure 7-15 of Wakerly, a rising edge behavior is illustrated wherein the flip flop changes its value upon detection of a rising signal source. The use of an edge triggered flip flop allows for the creation of a simple logic circuit that can be configured for various delays in triggering from low to high or high to low after receiving a signal.

Argument

Regarding the Examiner's rejection of independent claim 1, Applicant submits that the combination of Panwar in view of Wakerly fails to teach or suggest all of the elements of the Applicant's amended claim 1. Applicant submits that the cited art fails to teach of suggest the calculation of the number of called instructions with a microprocessor as set forth in amended claim 1. Applicant further submits that the cited art of Wakerly fails to teach the *edge detection of valid instructions* in accordance with the present invention. The cited Wakerly reference simply details the use of edged detection of a signal to control a change in output of a logic circuit. As stated on Page 540 of the Wakerly reference,

> "A positive edge triggered D flip-flop combines a pair of D latches as shown in Figure 7-15, to create a circuit that samples its D input and changes its Q outputs **only at the rising edge of a controlling CLK signal."**

Such language clearly indicated that the Wakerly art relates to logical circuitry and only uses edge detection associated with a variable logical signal for triggering the latches within the flip-flop. Furthermore, the flip flop of Wakerly continually triggers between logical states upon the detection of each new rising edge. The present application, in comparison used edge detection in conjunction with a bundled set of instructions to detect when the string of valid bits, corresponding to each valid instructions, transitions from high ("1") to low ("0"). When the edge detect circuit detects a "1" to "0" transition instruction processing by the edge detection circuit stops, as there is no longer a need to population count the number of valid bits in each slot in the bundle. Such detection of valid instructions, wherein the edge detection stop upon a detection of a first "1" to "0" transition (i.e. high to low), is clearly lacking in the cited art.

In light of the arguments set forth prior, Applicants submit that the cited art fails to render amended claim 1 obvious as urge the Examiner to pass amended claim 1 to allowance.

Independent claim 2 (upon which claims 3-5, 7-12 and 14-16 are dependent) discloses a method of calculating the number of valid instructions with a microprocessor including the steps of fetching a bundle of instructions and edge detecting valid instructions within the bundle. The Examiner has rejected independent claim 2, and those dependent claims which rely on

independent claim 2 for support, in view of Panwar and Wakerly. Applicant respectfully traverses this rejection on the basis that the cited art fails to teach or suggest each element of the amended claim 2. Applicants submit that the cited art, alone or in combination, fails to teach or suggest the calculation of the number of valid instructions within a microprocessor in accordance with amended claim 2. Furthermore, applicants submit that the alleged detection of valid instructions noted by the Examiner at column 12, lines 14-35 is only applicable to a method in which a main bundle of instructions if first split into a plurality of sub bundles. The detection of valid instruction under Panwar is based upon the assumption that, "an eight instruction main bundle contains two complex instructions at the third and sixth positions in the main bundle. Correspondingly, there are five sub-bundles." (Column 12, lines 2-5 of Panwar) Therefore, the detection of valid instruction within a bundle as set forth in amended claim 2is neither taught nor suggested by Panwar. Furthermore, as set forth prior, the Wakerly art simply details the use of edged detection of a signal to control a change in output of a logic circuit. Wakerly fails to teach or suggest the detection of valid instructions, but rather simply discloses the detection of a variable source signal and the control of an output based upon the conditions of the source signal.

Applicants further submits that dependent claims 3-5, 7-12 and 14-16 are further in condition for allowance by way of their nature as dependent claims. Furthermore, regarding the Examiner's rejection of claim 3, applicant submits that the shifting of at least one instruction is not taught or suggested by the cited art. As detailed by the Examiner, Panwar discloses the shifting of an instruction from the main bundle of instruction to a secondary sub bundle of instructions. The present invention, in contract, teaches the shifting of at least one instruction *within the bundle,* wherein it is not essential to transition an instruction from the bundle to a separate sub bundle in accordance with Panwar.

Regarding the Examiner's rejection to dependent claim 4, Applicant submits that the Panwar art cited by the Examiners fails to render teach or suggest the rotating at least one instruction *based at last in part on the number of valid instructions in the bundle*. Panwar, as detailed by the Examiner, discloses the shifting of an instruction from the middle of a *main bundle* to the top of a *sub bundle*. The cited art to Panwar fails to teach or suggest the rotation of at least one instruction within the bundle based in part on the number of valid instructions in the

bundle. In light of such arguments, Applicant respectfully submits that claim 4 is in condition for allowance.

In regards to the Examiner's objection to claim 5 of the pending application, Applicant submits that claim 5, as drafted, is in condition for allowance. The cited figures and language of Panwar detail the expanding of a main bundle of instruction into a plurality of sub-bundles, each sub bundle containing one type of instruction (i.e. Complex or non-complex). The creation of such sub-bundles is detailed in figure 5, as cited by the Examiner, as well as the text at Column 10, lines 6-12. The present invention, as noted in claim 5 details the *compressing* of a bundle of instructions, as detailed in the specification, such that all the valid instructions, and corresponding valid bits, are compressed at the "top" of the bundle. Such a compression is illustrated in Figure 6 of the pending application. As Panwar fails to teach or suggest the compression of a bungle of instruction in accordance with the present invention, Applicant respectfully submits that claim 5 is in condition for allowance. Applicant further submits that claim 7, which details the compressing of the bundle of instructions based in part on the number of valid instructions is neither taught nor suggested by Panwar in light of the argument set forth prior detailed the expansion of a bundle of instructions under Panwar. In light of such arguments, Applicant urges the Examiner to pass claims 5 and 7 to allowance.

Independent claim 8 is further rejected as being obvious in light of Panwar in view of Wakerly. Applicant respectfully submits that the combination of Panwar in view of Wakerly fails to teach or suggest all of the elements of the Applicant's amended claim 8. Applicant submits that the Panwar art, as noted by the Examiner, fails to teach or suggest the use of edge detection. Furthermore, Applicant submits that the Wakerly art fails to teach or suggest the use of edge detection to detect the number of valid instructions in accordance with the present invention. As set forth prior, the Wakerly reference simply details the use of edged detection of a signal to control a change in output of a logic circuit. Furthermore, the flip flop of Wakerly continually triggers between logical states upon the detection of each new rising edge. The present application, in comparison used edge detection in conjunction with a bundled set of instructions to detect when the string of valid bits, corresponding to each valid instructions, transitions from high ("1") to low ("0"). Such detection of valid instructions, wherein the edge detection stop upon a detection of a first "1" to "0" transition (i.e. high to low), is clearly lacking

in the cited art. In light of such arguments, Applicant respectfully submits that pending claim 8 is in condition for allowance as drafted.

The Examiner has additionally rejected dependent claims 12, and 14-16 as being obvious in light of Panwar in view of Wakerly. Applicant submit that dependent claims 12, and 14-16, in view of the argument of above in regards to independent claim are in condition for allowance by their very nature as dependent claims.

Putting forth similar arguments as those directed toward claim 5, Applicant submits that Panwar fails to render claim 12 obvious. As set forth prior, Panwar *expands* the main bundle of instructions into a group of sub bundles, which is in direct contrast o the *compressing* of the instructions after the complex instructions of the pending application. Applicant therefore asks the Examiner to pass claim 12 to allowance.

In regards to the Examiner's objection to claim 14, Applicant submits that the cited art fails to teach or suggest the execution of instructions which occur prior to complex instruction during a first clock cycle. As evidenced by the language cited by the Examiner at column 2, lines 35-38, "instructions therefore are processed in the most efficient manner within the processor, generally within a minimum number of clock cycles." The cited art, however, fails to teach or suggest the execution of those instructions prior to the complex instruction in a first clock cycle. Furthermore, the cited language at column 6, lines 59-64, details the execution of instructions as soon as instruction dependencies have been satisfied into an appropriate unit,, such as an integer execution unit, graphical unit or floating point unit, but fails to teach or suggest the execution of the non-complex instructions during a first clock cycle in accordance with the present invention. Additionally, the element of executing the complex instruction during a second clock cycle, as detailed din claim 15 of the present invention, is not rendered obvious by the cited art. As set forth prior, the cited art fails to detail the execution sequence in relation to a clock cycle by which complex and non complex instructions are executed. The language cited by the Examiner, merely details the execution of various instructions using broad generalities such as "mot efficient manner" but fails to teach or suggest the manner by which complex and non-complex instructions should execute in accordance it he the present invention. Additionally, in regards to the objection to claim 16, Applicant submits that the shifting of an

instruction within an instruction bundle in relation to the execution of non-complex and complex instruction is neither taught nor suggested by the Panwar art. As set forth prior, Panwar discloses the shifting of an instruction from a main bundle into a sub bundle such that various types of instructions can be executed in various orders. The present invention, as recited in claim 16, in comparison teaches the shifting of an instruction *within an instruction bundle*, as opposed to a sub-bundle such as Panwar. In light of the arguments set forth prior, Applicants respectfully request that the Examiner pass claims 14, 15 and 16 to allowance.

Independent claim 17 is further rejected in view of Panwar in light of Wakerly. Applicant submits that claims 17, as amended, is in condition for allowance. As set forth in the arguments prior, Applicant submits that the Panwar art fails to teach or suggest the identification of a complex instruction within an instruction bundle and the execution of all valid instructions in the bundle located prior to the complex instruction, followed by the execution of the complex instruction during a second clock cycle. As noted by the Examiner in the cited language of Panwar, instructions of varying types under Panwar are identified and separated into sub bundles, such that each sub bundle may individually be executed. Furthermore, Panwar fails to teach or suggest the shifting of instruction *within the bundle* but rather utilizes numerous sub bundles for separating instruction types. Finally, as set forth prior, the edge detection technique of Wakerly, for use in a logical flip flop device, fails to teach or suggest the edge detection technique for use in detection of valid instructions as presented in the pending application. In light of such arguments, Applicant respectfully asks that the Examiner withdraw his rejection to claim 17 and pass claim 17 to allowance.

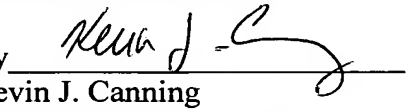
Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Applicant further submits that the newly introduced claims are simply the apparatus claim equivalents to the method claims currently pending in the application. These newly introduced claims introduce no new matter and Applicant submits are fully supported by the specification. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-143 (P6594) from which the undersigned is authorized to draw.

Dated: October 15, 2004

Respectfully submitted,

By 

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Amendments to the Drawings:

Figures 3, 6A and 6B of the pending application have been amended to illustrates every feature of the invention, as requested by the Examiner in the pending Office Action. Applicant submits that these amended figures introduce no new mater and adequately overcome the Examiner's objection.

In particular, Figure 3 has been amended to more clearly illustrate the passage of an instruction through an instruction pipeline. Additionally, Figure 6A and 6B have been amended to illustrate the use of an edge detection circuit 91 with the present invention.

In view of such amendments, Applicant respectfully submits that the drawings are in compliance and serve to adequately illustrate every feature of the invention specified in the claims.

FIG. 3

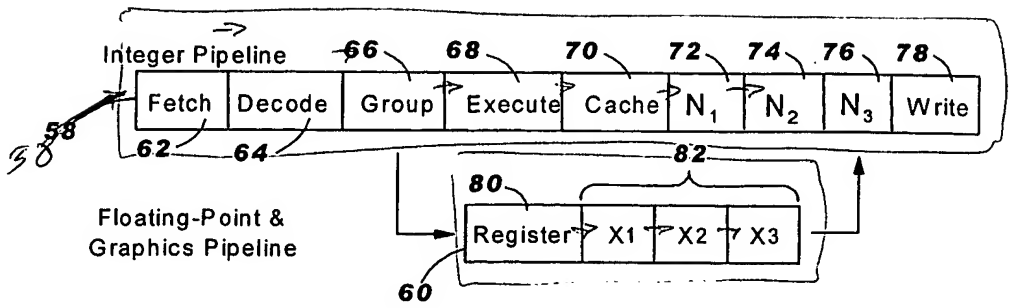

FIG. 4 delete

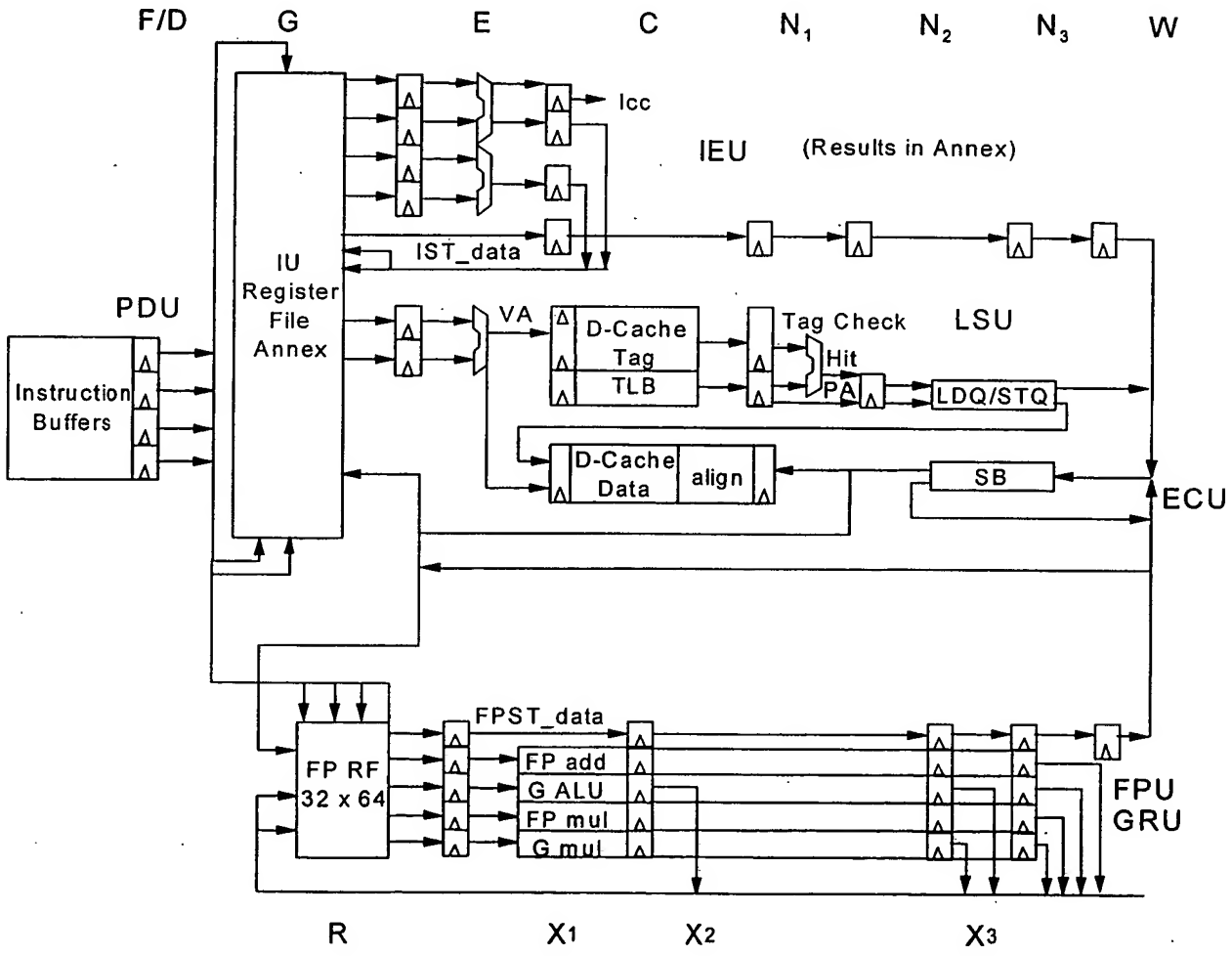

FIG. 6A

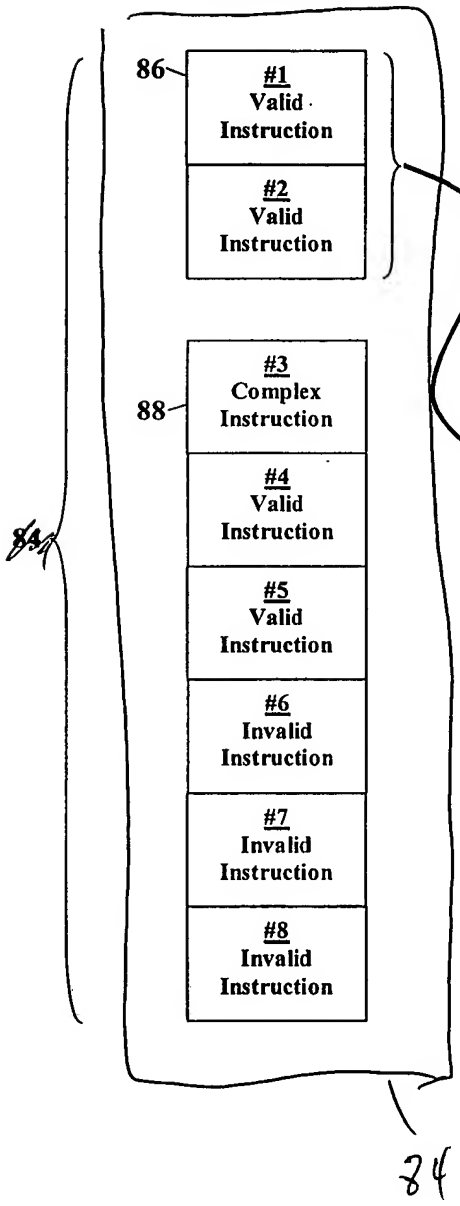

FIG. 6B